nexperia

Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of http://www.nxp.com, http://www.philips.com/ or http://www.semiconductors.philips.com/, use **http://www.nexperia.com**

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:
- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved
Should be replaced with:
- **© Nexperia B.V. (year). All rights reserved**.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

Package lead inductance considerations in high-speed applications

AN212

Authors: Stephen C. Hinkle, Jeffrey A. West

INTRODUCTION

A circuits become faster, more concern needs to be focused on packaging and interconnects in order to fully utilize device performance. One area of concern is with the package leads between the chip and the board environment. The current flowing into or out of an integrated circuit is conducted through a lead frame trace and bonding wire connecting the integrated circuit to outside circuitry. these leads are circuit elements, inductors, and have a definite effect on the circuit performance because they generate noise in high-speed applications.

Inductance is the measure of change in the magnetic field surrounding a conductor resulting form the variation of the current flowing through the conductor. The change in current through the inductor induces a counter electromotive force, EMF, which opposes that change in current.

An example is a buffer driver discharging a 50pF load. At a switching rate of about 3V in 2ns, the current generated by discharging that capacitor at that rate is:

$$I = C\frac{dV}{dt} \simeq 50pF \cdot \frac{3v}{2ns} = 75mA.$$

All this current flows through the ground lead of the package. Changing the current through this lead generates a ground lead voltage or ground bounce. A typical lead inductance has been measured to be about 10nH. Switching 75mA through a ground lead with an inductive value of 10nH causes a ground bounce of about:

$$V = L\frac{dI}{dt} \simeq 10nH \cdot \frac{75mA}{1ns} = 750mV.$$

Figure 1 illustrates the current surge and ground bounce during switching. This was modeled using the equations:

$$V(t) = \frac{3V}{1 + E^{(t - t_O)/K}}$$

$$I_C(t) = C\frac{dV(t)}{dt}$$

$$V_L(t) = L\frac{dI_C(t)}{dt} = LC\frac{D^2V(t)}{dt^2}$$

If more than one output is switched at a time, this ground bounce can get very large. Changing the ground reference on the chip can have significant effects on circuit performance. A V_{CC} bounce can also be calculated when the 50pF load capacitors are being charged and can also have serious effects on circuit performance.

Some of the problems caused by package lead inductance are:

1. Adding delay through buffer parts
2. Changing the state of flip-flop parts
3. Output glitching on unswitched outputs
4. Circuit oscillations.

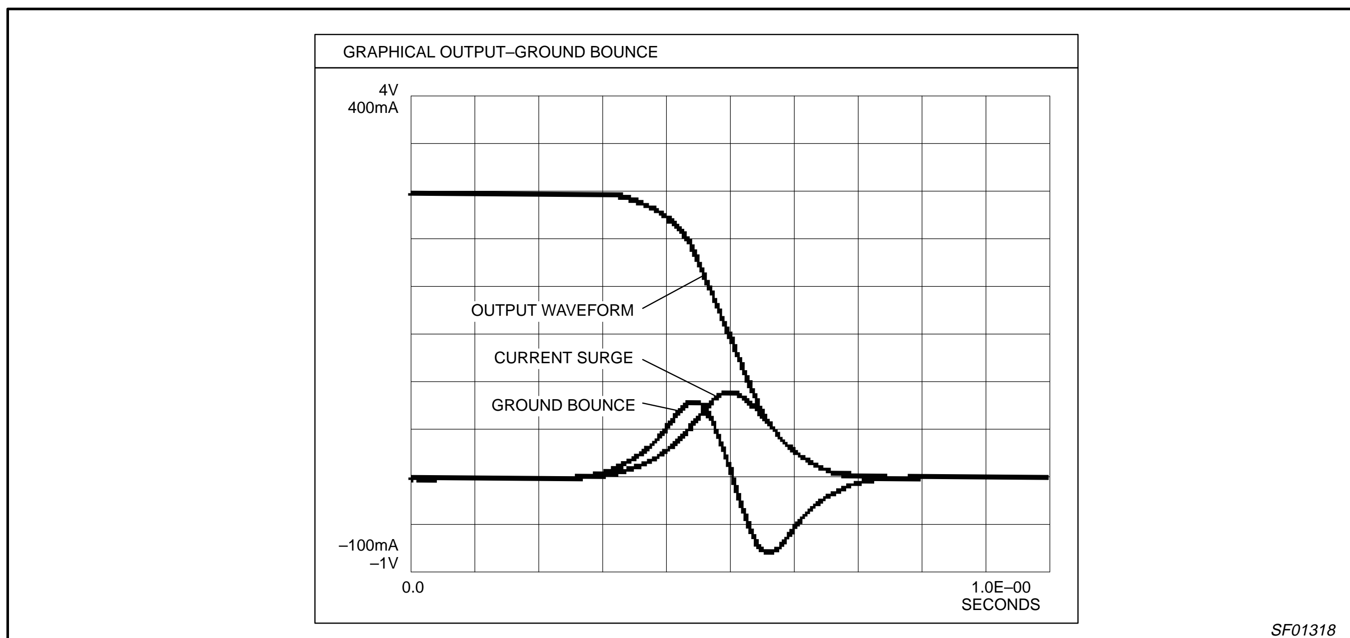

Figure 1.

GENERAL PROBLEMS ASSOCIATED WITH GROUND BOUNCE IN HIGH-SPEED CIRCUITS

Adding Delay Through Buffer Parts

Delay through a buffer part is not only a function of the gate itself but is also a function of how many gates in the package are switching at once. Switching more than one output at a time adds to the current being forced through the ground lead of the package. the ground potential seen by the chip rises because of the lead inductance. This rise in ground potential raises the threshold of the gate and tends to turn the gate back OFF slowing the discharge rate of the load capacitor. The gate does not finish switching until the ground bounce settles out.

Figure 2 shows an example of a buffer connected to a test load. Probing on the ground pad, V_G, shows the effect ground lead inductance has on the ground pad potential.

Figures 3 and 4 show the ground and V_{CC} bounce during switching on a 74F240 Buffer. The effect of ground bounce on this part is to slow the propagation delays from 3ns with only one output switching to 5ns with all 8 outputs switching at once. AC specifications are usually generated with only one gate switching at a time. For example, the 74F240 t_{PHL} limits are 2.0ns minimum, 3.5ns typical and 4.7ns maximum. Therefore, when using AC specifications based on single gate switching, a derating factor for multiple switching should be used. A derating factor of 250 to 300ps per output switching has been suggested as a reasonable number and some customers are using this i their internal specifications.

Integrated Circuits Containing Flip-Flops

Integrated circuits containing flip-flops might be seriously affected by inductive ground bounce because of the possibility of the flip-flops changing states. To explore this effect, the 74F374, and Octal D-type Flip-Flop, was analyzed by comparing test results from the conventional corner mount V_{CC} and ground package to that of a side mount V_{CC} and ground version. A test setup as used where alternate 1's and 0's were clocked into seven of the eight flip-flops to obtain simultaneous output switching and worst case ground bounce. The eighth flip-flop input was held at a DC bias of 2.0V. This should result in its output being held at a constant 1 level.

Figure 5 shows the corner mount results. The ground bounce is sufficient to couple the output of the eighth flip-flop (Q7) to less than 2.0V during the transition of the other seven outputs represented by Q6. The output then charges to a marginal V_{OH} level.

Figure 6 shows the results from the side mount version. Output glitching during the transition of the other seven outputs is still present, but due to the approximately 50% reduction in lead inductance over the corner mount version, the output is allowed to charge back to its original V_{OH} level.

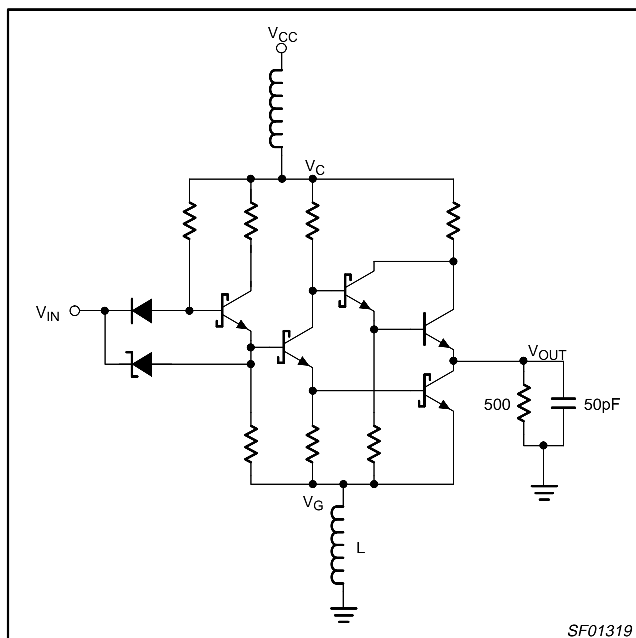

Figure 2.

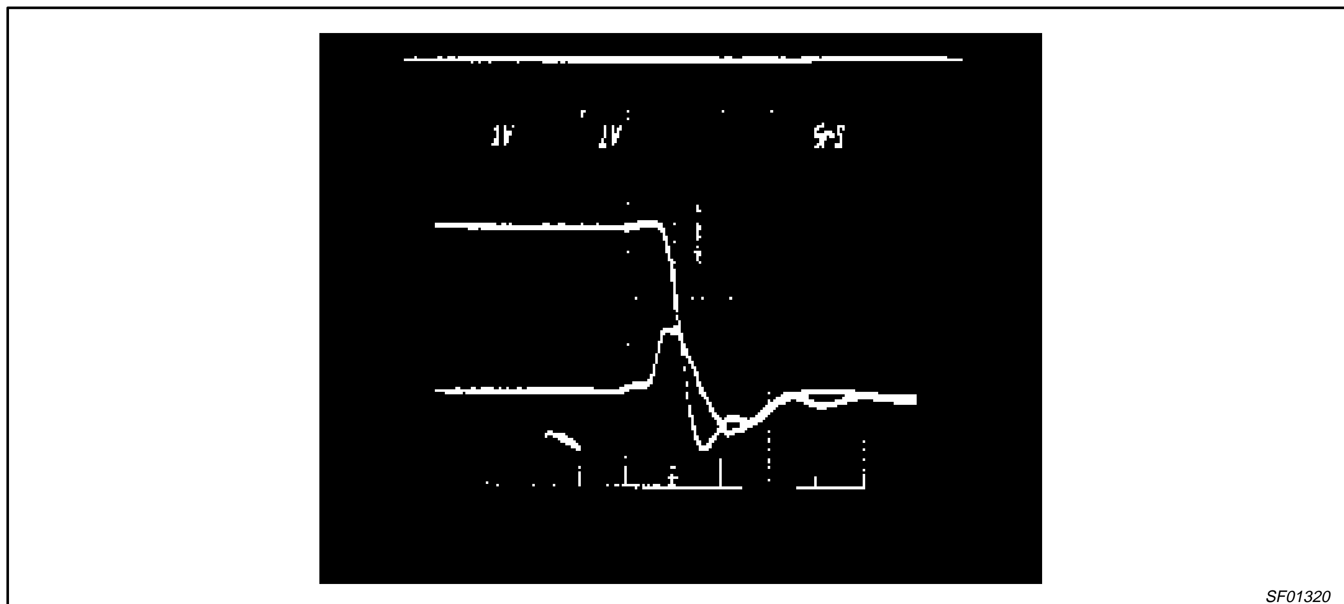

Figure 3.

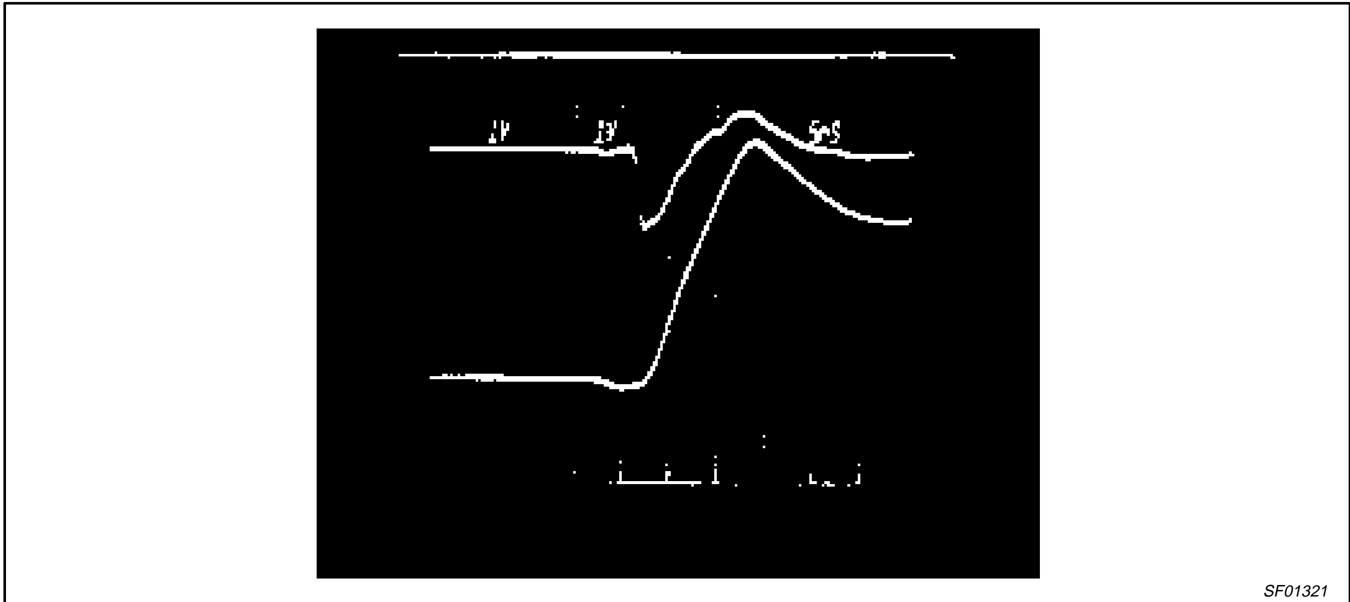

Figure 4.

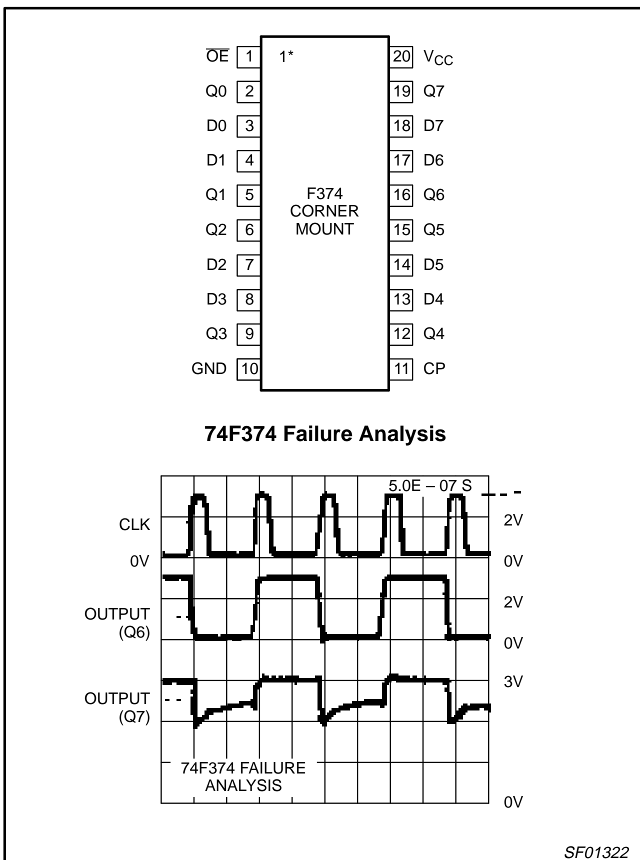

Figure 5.

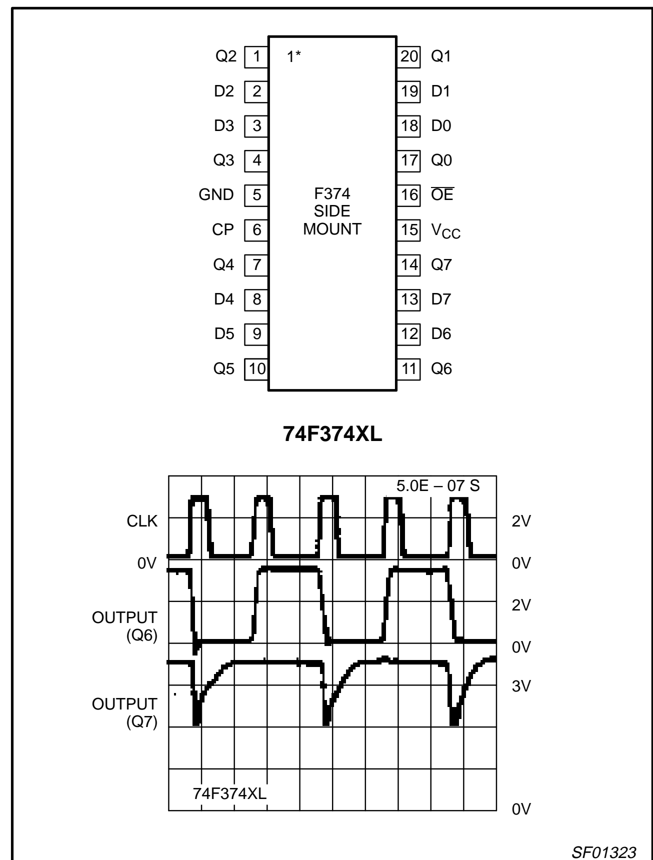

Figure 6.

Output Glitching During Multiple Switching

In some cases, the effects of ground bounce can be minimized if properly taken into consideration during the design and layout of the integrated circuit. Note in Figure 7, the glitch that was present on the output of the 74F11, a triple 3-input AND gate, during an early transition of the other two outputs. A newer version of the 74F11 is shown in Figure 8. Note that the glitch has been greatly minimized.

Circuit Oscillations

A fourth area of concern is the possibility of circuit oscillations during slow input transitions through threshold. This would be of importance if the delay through the part is on the order of the natural period of the ground inductance and the load capacitance.

During testing, a particular problem has been seen when the inputs are driven by a power supply by way of a cable. Because there is a delay through the cable, it takes time for the power supply to sense a change in the impedance at the input near threshold. This delay sets up oscillations between the power supply and the input of the part when the input is held near threshold.

Inductance Measurements and Verification

To verify that lead inductance caused these problems, the lead inductance was measured and circuit simulations done to show circuit behavior. Measurement of lead inductance was accomplished using an HP S-parameter test set. These measured values of lead inductance were used in a circuit simulation program. The results of the simulation show voltage and current wave forms similar to the measured waveforms.

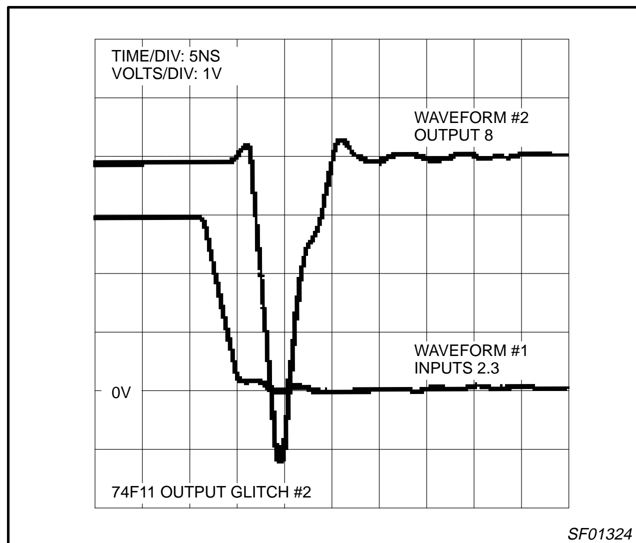

Figure 7.

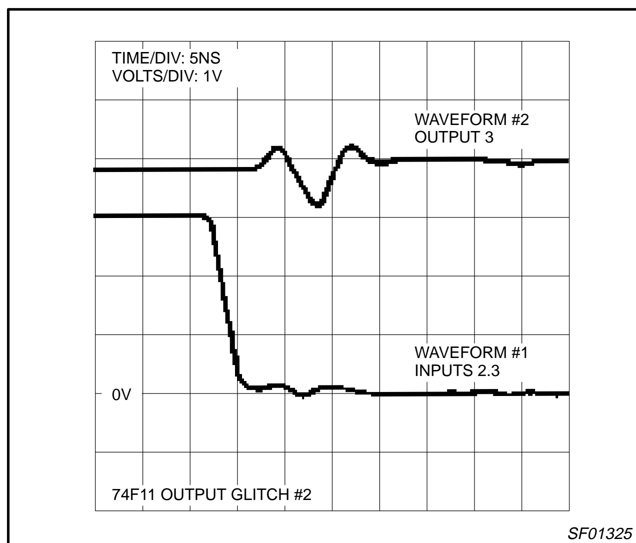

Figure 8.

Derivation of the S-parameter Method

The general form for voltage and current along a transmission line is:

$\overline{V}(z) = V^+ e^{-\gamma z} + V^- e^{\gamma z}$
$I(z) = I^+ e^{-\gamma z} - I^- e!s$

Where V^+, V^-, I^+, I^- are constants, usually complex, determined by the boundary conditions, z is the distance from the load and gamma (γ) is a complex term involving a real or loss term and an imaginary or phase shift term.

$$\gamma = \propto + j\beta$$

$$\gamma \simeq 1/2(R\sqrt{C/L} + G\sqrt{L/C}) + j\omega\sqrt{LC}.$$

Considering the lossless case where R = 0 and G = 0, $\gamma = j\beta$ and only results in a phase shift. The equations for voltage and current then become:

$$\overline{V}(z) = V^+ e^{-j\beta z} + V^- e^{j\beta z}$$

$$\overline{I}(z) = I^+ e^{-j\beta z} - I^- e^{j\beta z}$$

To find Z_1 set z = O. (See Figure 9).

$$\overline{Z}_1 = \overline{V}_1/\overline{I}_1 = (V^+ + V^-)/(I^+ - I^-)$$

since, $I^+ = V^+/Z_0$ and,

$I^- = V^-/Z_0$,
$Z_1 = (V^+ + V^-)/(V^-/Z_0 - V^+/Z_0)$, or,

$$\overline{Z}_1 = Z_0 \frac{1 + V^-/V^+}{1 - V^-/V^+}$$

V^-/V^+ is called the reflection coefficient and is usually complex,

$$\Gamma = V^-/V^+.$$

The impedance at the load then becomes:

$$\overline{Z}_1 = Z_0 \frac{1+\Gamma}{1-\Gamma}$$

On the S-parameter test set, the magnitude of the reflection coefficient, $|\Gamma|$, is measured in dB at a particular angle,

$$\Gamma_{real} = 10^{(|\Gamma\, dB|/20)} \angle \theta.$$

For an inductor,

$$\overline{Z}_1 = Z_0 \frac{1+\Gamma}{1-\Gamma} = R + j\omega L$$

usually $R \simeq 0$ and L can be solved for directly.

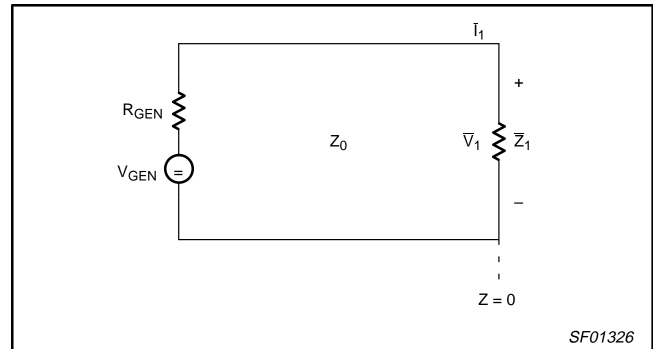

Figure 9.

Example

A 16-pin package measuring from pin 8 to 16 has a reflection coefficient $\Gamma_{dB} = -0.5 \angle 162°$, Z_0 of the system is 50Ω and the measurement frequency is 50MHz.

$$\Gamma_{dB} = -0.5 \angle 162°$$

$$\Gamma_{real} = 0.944 \angle 162° = -0.898 + j0.292$$

$$\overline{Z}_1 = Z_0 \frac{1+\Gamma}{1-\Gamma} = 50 * \frac{0.102 + j0.292}{1.898 - j0.292}$$

$$= 50 * \frac{0.309 \quad 70.7°}{1.920 \quad -8.74°}$$

$$= 8.05 \angle 79°$$

$$\overline{Z}_1 = 1.475 + j7.914$$

$$L = 7.914/(2\pi * 50MHz) = \underline{25.19nH}$$

Alternately, using the approximation R = 0, so $|Z_1| = \omega L$:

$$L = \frac{8.05}{2\pi * 50MHz} = \underline{25.62nH}$$

Three packages were used to measure lead inductance, a 16-pin CERDIP, a 24-pin CERDIP and a 24-pin skinny CERDIP. V_{CC} and ground were double bonded to an 80×80 mil blank die. Table 1 shows the results of the measurements.

These values are the total inductance V_{CC} to ground. Each lead inductance would be about one half these numbers.

Table 1.

PACKAGE	REFLECTION COEFFICIENT	INDUCTANCE
16-pin (300mil-wide)		
8 to 16	–0.50 ∠ 162°C	25.62nH
4 to 12	–0.32 ∠ 172°C	11.51nH
24-pin (600mil-wide)		
12 to 24	–0.56 ∠ 157°C	32.78nH
6 to 18	–0.29 ∠ 157°C	18.33nH
24-pin (300mil-wide)		
12 to 24	–0.47 ∠ 160°C	28.39nH
6 to 18	–0.34 ∠ 170°C	14.27nH

Simulation of Measured Values

Both ground and V_{CC} bounce for the 74F240 were simulated using the inductive values measured. The results were similar to the measured data of the 74F240. Figures 3 and 4. The simulation of the 74F240 is shown in Figure 10. this shows the pad V_{CC}, the pad ground (V_G) and the inputs (V_{IN}) and output (V_{OUT}) when all 8 buffers are switched simultaneously.

SUMMARY

A major contributor to noise in High-speed circuits is package lead inductance. Integrated circuits are packaged with lead frame traces and bonding wire. These leads act as inductors. Voltage generated across these leads follow the law:

$$V = L\frac{di}{dt}$$

This represents noise to an integrated circuit chip and can cause performance degradation. The faster the switching rates become,, the more lead inductance can affect circuit performance.

As circuits become faster, more care should be taken in packaging and chip layout. In some cases like the 74F11, a better layout can help remove potential problems but in most cases like the 74F240, the noise is strictly a function of the package. Care should be taken in integrated circuit packages to minimize lead lengths. Side mount V_{CC} and ground pins, smaller packages such as the surface mounted SO, and High levels of board integration are fa few possibilities which would help minimize lead lengths.

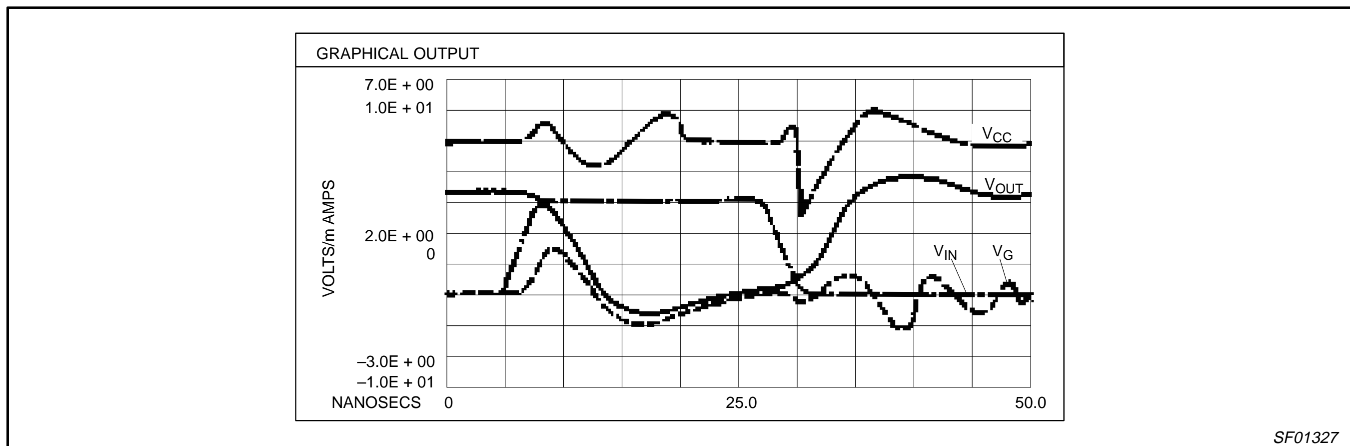

Figure 10.